

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An active matrix type display device comprising:
a plurality of pixels arranged in matrix formed over a substrate;
a driver circuit for driving the plurality of pixels over said substrate, said driver circuit including at least one buffer circuit;
at least two transistors in said at least one buffer circuit;
a common gate electrode adjacent to channel-forming regions of said at least two transistors;
a ~~common~~ source electrode connected with source regions of said at least two transistors; and
a ~~common~~ drain electrode connected with drain regions of said at least two transistors,
wherein said at least two transistors are connected with each other in parallel through said common gate electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode,
wherein said channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively, and
wherein said channel-forming regions are formed in contact with a same insulating surface, and
wherein said at least two separate semiconductor layers are arranged in a channel width direction.

2. (Currently Amended) An active matrix type display device comprising:
a plurality of pixels arranged in matrix formed over a substrate;

a driver circuit for driving the plurality of pixels over said substrate;
at least two transistors in said driver circuit;
a common gate electrode adjacent to channel-forming regions of said at least two transistors;
a ~~common~~ source electrode connected with source regions of said at least two transistors; and
a ~~common~~ drain electrode connected with drain regions of said at least two transistors,
wherein said at least two transistors are connected with each other in parallel through said common gate electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode,
wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively, and wherein said channel-forming regions are formed in contact with a same insulating surface, and
wherein said at least two separate semiconductor layers are arranged in a channel width direction.

3.-10. (Canceled)

11. (Previously Presented) The device of claim 1 wherein said active matrix type display device comprises a memory.

12. (Previously Presented) The device of claim 1 wherein said active matrix type display device comprises a decoder.

13. (Previously Presented) The device of claim 1 wherein said active matrix type display device comprises a display system.

14. (Previously Presented) The device of claim 2, wherein said active matrix type display device comprises a memory.

15. (Canceled)

16. (Previously Presented) The device of claim 2 wherein said active matrix type display device comprises a display system.

17.-37. (Canceled)

38. (Previously Presented) The device of claim 58 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

39. (Previously Presented) The device of claim 58 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

40. (Previously Presented) The device of claim 59 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

41. (Previously Presented) The device of claim 59 wherein ratio (I/I_0) between a

Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

42.-57. (Canceled)

58. (Previously Presented) The device of claim 1 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

59. (Previously Presented) The device of claim 2 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

60.-70. (Canceled)

71. (Previously Presented) The device of claim 1 wherein said active matrix type display device is a liquid crystal display device.

72. (Previously Presented) The device of claim 2 wherein said active matrix type display device is a liquid crystal display device.

73.-77. (Canceled)

78. (Previously Presented) The device of claim 1 wherein said channel-forming regions have point defects.

79. (Previously Presented) The device of claim 2 wherein said channel-forming regions have point defects.

80.-99. (Canceled)

100. (Previously Presented) The device of claim 1, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, respectively, and contains oxygen at a concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less.

101. (Previously Presented) The device of claim 2, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of $5 \times 10^{18} \text{ cm}^{-3}$ or less, respectively, and contains oxygen at a concentration of $5 \times 10^{19} \text{ cm}^{-3}$ or less.

102.-121. (Canceled)

122. (Currently Amended) An active matrix type display device comprising:
a plurality of pixels over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, wherein said driver circuit comprises a buffer circuit, wherein said buffer circuit comprises a first thin film transistor and a second thin film transistor, wherein said first thin film transistor comprises a first semiconductor layer and said second thin film transistor comprises a second semiconductor layer, and wherein said first semiconductor layer and said second semiconductor layer are formed in contact with a same insulating surface;

a common gate electrode adjacent to said first semiconductor layer and said second semiconductor layer;

a ~~common~~ source electrode electrically connected with said first semiconductor layer and said second semiconductor layer; and

a ~~common~~ drain electrode electrically connected with said first semiconductor layer and said second semiconductor layer,

wherein said first thin film transistor and said second thin film transistor are connected in parallel with each other through said common gate electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode,

wherein said first semiconductor layer and said second semiconductor layer are separately provided with each other, and

wherein said first semiconductor layer and said second semiconductor layer are arranged in a channel width direction.

123. (Currently Amended) The device of claim 122, wherein said ~~common~~ source electrode and said ~~common~~ drain electrode are directly in contact with said first semiconductor layer and said second semiconductor layer.

124. (Currently Amended) The device of claim 122, wherein said common gate electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode extend in parallel with each other.

125. (Previously Presented) The device of claim 122, wherein said common gate electrode is formed over said first semiconductor layer and said second semiconductor layer.

126. (Previously Presented) The device of claim 122, wherein said first semiconductor layer and said second semiconductor layer comprise monocrystalline silicon.

127. (Previously Presented) The device of claim 122, wherein said active matrix type display device is a liquid crystal display device.

128. (Currently Amended) An active matrix type display device comprising:
a plurality of pixels over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, wherein said driver circuit comprises a first thin film transistor and a second thin film transistor, wherein said first thin film transistor comprises a first semiconductor layer and said second thin film transistor comprises a second semiconductor layer, and wherein said first semiconductor layer and said second semiconductor layer are formed in contact with a same insulating surface;

a common gate electrode adjacent to said first semiconductor layer and said second semiconductor layer;

a ~~common~~ source electrode electrically connected with said first semiconductor layer and said second semiconductor layer; and

a ~~common~~ drain electrode electrically connected with said first semiconductor layer and said second semiconductor layer,

wherein said first thin film transistor and said second thin film transistor are connected in parallel with each other through said common gate electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode,

wherein said first semiconductor layer and said second semiconductor layer are separately provided with each other, and

wherein said first semiconductor layer and said second semiconductor layer are arranged in a channel width direction.

129. (Currently Amended) The device of claim 128, wherein said ~~common~~ source electrode and said ~~common~~ drain electrode are directly in contact with said first semiconductor layer and said second semiconductor layer.

130. (Currently Amended) The device of claim 128, wherein said common gate

electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode extend in parallel with each other.

131. (Previously Presented) The device of claim 128, wherein said common gate electrode is formed over said first semiconductor layer and said second semiconductor layer.

132. (Previously Presented) The device of claim 128, wherein said first semiconductor layer and said second semiconductor layer comprise monocrystalline silicon.

133. (Previously Presented) The device of claim 128, wherein said active matrix type display device is a liquid crystal display device.

134. (Currently Amended) An active matrix type display device comprising:
a plurality of pixels over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, wherein said driver circuit comprises a buffer circuit, wherein said buffer circuit comprises a first thin film transistor and a second thin film transistor,

wherein said first thin film transistor comprises a first semiconductor layer and said second thin film transistor comprises a second semiconductor layer, and wherein said first semiconductor layer and said second semiconductor layer are formed in contact with a same insulating surface;

a common gate electrode adjacent to said first semiconductor layer and said second semiconductor layer;

a ~~common~~ source electrode electrically connected with said first semiconductor layer and said second semiconductor layer; and

a ~~common~~ drain electrode electrically connected with said first semiconductor

layer and said second semiconductor layer,

wherein said first thin film transistor and said second thin film transistor are connected in parallel with each other through said common gate electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode,

wherein said first semiconductor layer and said second semiconductor layer are not in direct contact with each other, and

wherein said first semiconductor layer and said second semiconductor layer are arranged in a channel width direction.

135. (Currently Amended) The device of claim 134, wherein said ~~common~~ source electrode and said ~~common~~ drain electrode are directly in contact with said first semiconductor layer and said second semiconductor layer.

136. (Currently Amended) The device of claim 134, wherein said common gate electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode extend in parallel with each other.

137. (Previously Presented) The device of claim 134, wherein said common gate electrode is formed over said first semiconductor layer and said second semiconductor layer.

138. (Previously Presented) The device of claim 134, wherein said first semiconductor layer and said second semiconductor layer comprise monocrystalline silicon.

139. (Previously Presented) The device of claim 134, wherein said active matrix type display device is a liquid crystal display device.

140. (Currently Amended) An active matrix type display device comprising:

a plurality of pixels over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, wherein said driver circuit comprises a first thin film transistor and a second thin film transistor,

wherein said first thin film transistor comprises a first semiconductor layer and said second thin film transistor comprises a second semiconductor layer, and wherein said first semiconductor layer and said second semiconductor layer are formed in contact with a same insulating surface;

a common gate electrode adjacent to said first semiconductor layer and said second semiconductor layer;

a ~~common~~ source electrode electrically connected with said first semiconductor layer and said second semiconductor layer; and

a ~~common~~ drain electrode electrically connected with said first semiconductor layer and said second semiconductor layer,

wherein said first thin film transistor and said second thin film transistor are connected in parallel with each other through said common gate electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode,

wherein said first semiconductor layer and said second semiconductor layer are not in direct contact with each other, and

wherein said first semiconductor layer and said second semiconductor layer are arranged in a channel width direction.

141. (Currently Amended) The device of claim 140, wherein said ~~common~~ source electrode and said ~~common~~ drain electrode are directly in contact with said first semiconductor layer and said second semiconductor layer.

142. (Currently Amended) The device of claim 140, wherein said common gate electrode, said ~~common~~ source electrode, and said ~~common~~ drain electrode extend in

parallel with each other.

143. (Previously Presented) The device of claim 140, wherein said common gate electrode is formed over said first semiconductor layer and said second semiconductor layer.

144. (Previously Presented) The device of claim 140, wherein said first semiconductor layer and said second semiconductor layer comprise monocrystalline silicon.

145. (Previously Presented) The device of claim 140, wherein said active matrix type display device is a liquid crystal display device.